○ TRANSMISSION BIT ORDER (D0 TO D9 SHOW TRANSMISSION DATA, C4 TO C0 SHOW CRC BITS)

CONVENTIONAL POSTPOSITION : D9,D8,D7,D6,D5,D4,D3,D2,D1,D0,C4,C3,C2,C1,C0

PREPOSITION : C4,C3,C2,C1,C0,D9,D8,D7,D6,D5,D4,D3,D2,D1,D0

FIG.1A

○ RECEIVED DATA BIT AND RECEIVED CRC BIT
(WHEN DETECTING A POSITION WHERE THE NUMBER OF BITS IS SMALLER BY ONE FROM THE CORRECT RATE POSITION)

CONVENTIONAL POSTPOSITION: DATA = D9,D8,D7,D6,D5,D4,D3,D2,D1 CRC=D0,C4,C3,C2,C1

PREPOSITION: DATA = D9,D8,D7,D6,D5,D4,D3,D2,D1 CRC=C4,C3,C2,C1,C0

FIG.1B

○TRANSMISSION BIT ORDER (D0 TO D9 SHOW TRANSMISSION DATA, C4 TO C0 SHOW CRC BITS)

CONVENTIONAL POSTPOSITION : D9,D8,D7,D6,D5,D4,D3,D2,D1,D0,C4,C3,C2,C1,C0

NEW POSTPOSITION : D9,D8,D7,D6,D5,D4,D3,D2,D1,D0,C0,C1,C2,C3,C4

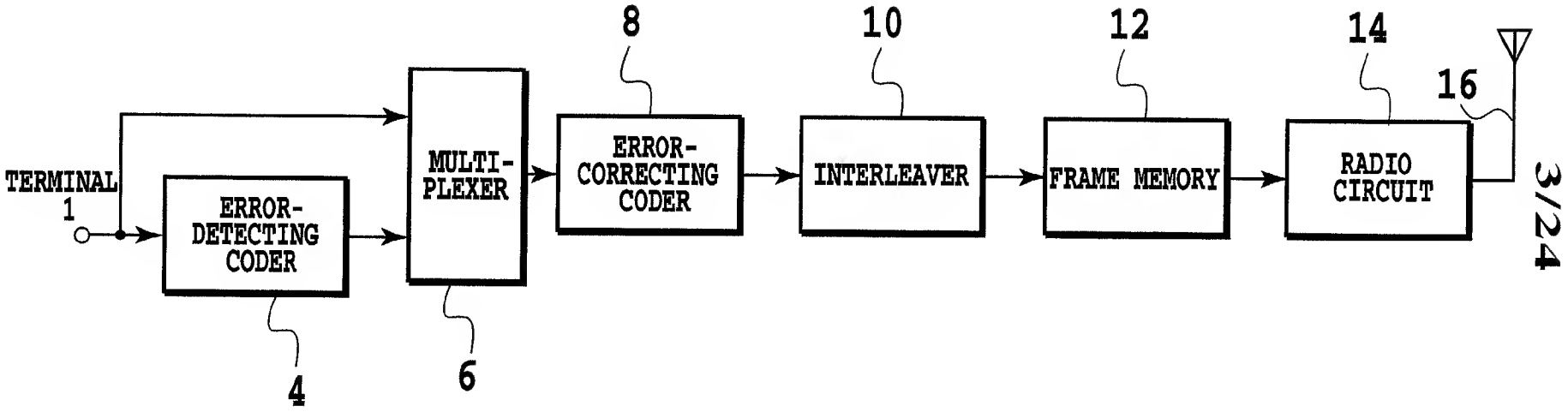
FIG.2A

○RECEIVED DATA BIT AND RECEIVED CRC BIT
(WHEN DETECTING A POSITION WHERE THE NUMBER OF BITS IS SMALLER BY ONE FROM THE CORRECT RATE POSITION)

CONVENTIONAL POSTPOSITION: DATA =D9,D8,D7,D6,D5,D4,D3,D2,D1 CRC=D0,C4,C3,C2,C1

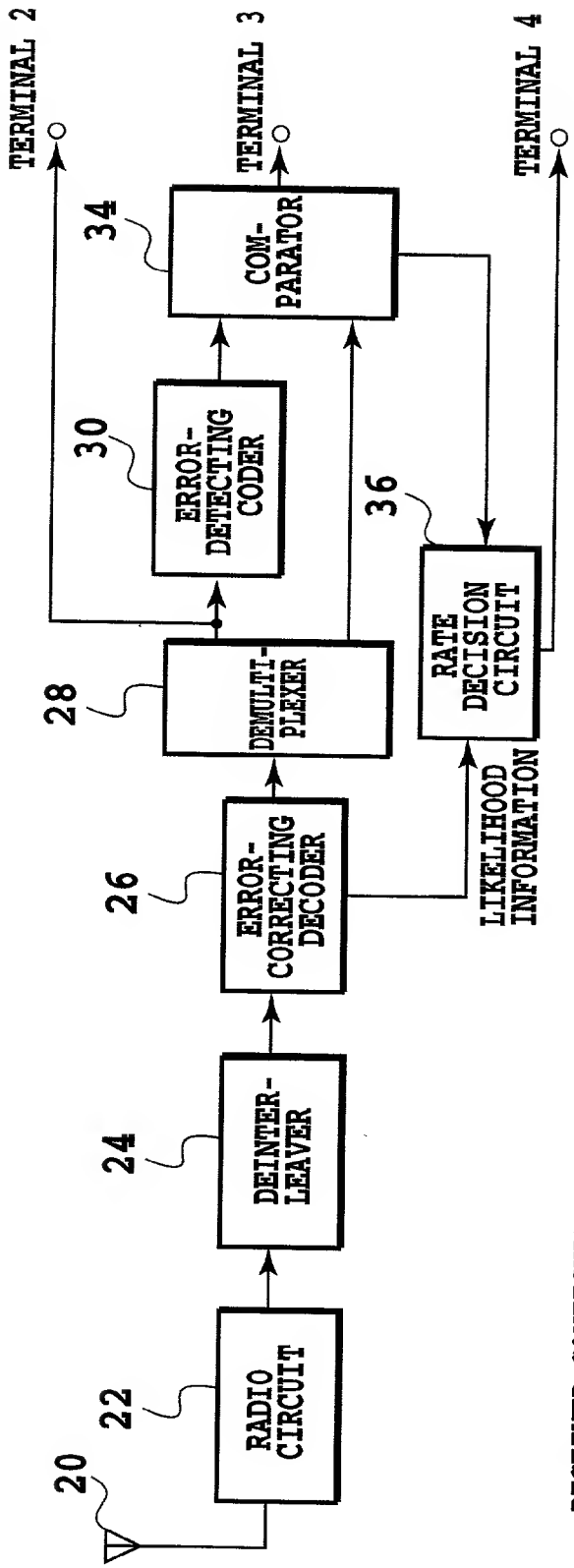
NEW POSTPOSITION: DATA =D9,D8,D7,D6,D5,D4,D3,D2,D1 CRC=D0,C0,C1,C2,C3

FIG.2B



TRANSMITTER CONFIGURATION

FIG.3A



RECEIVER CONFIGURATION

FIG.3B

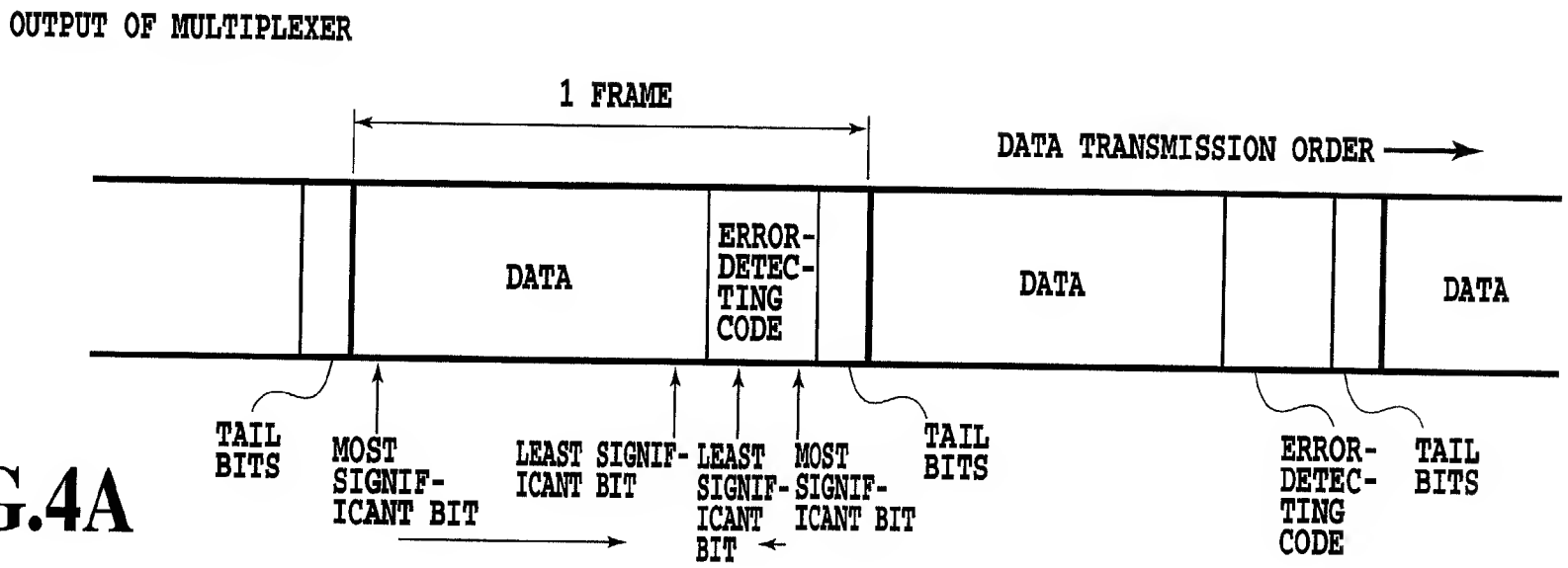

OUTPUT OF MULTIPLEXER
1 FRAME
DATA TRANSMISSION ORDER
DATA
ERROR-DETEC-TING CODE
DATA
DATA
TAIL BITS
MOST SIGNIF-ICANT BIT
LEAST SIGNIF-ICANT BIT
LEAST SIGNIF-ICANT BIT
MOST SIGNIF-ICANT BIT
TAIL BITS
ERROR-DETEC-TING CODE
TAIL BITS

FIG.4A

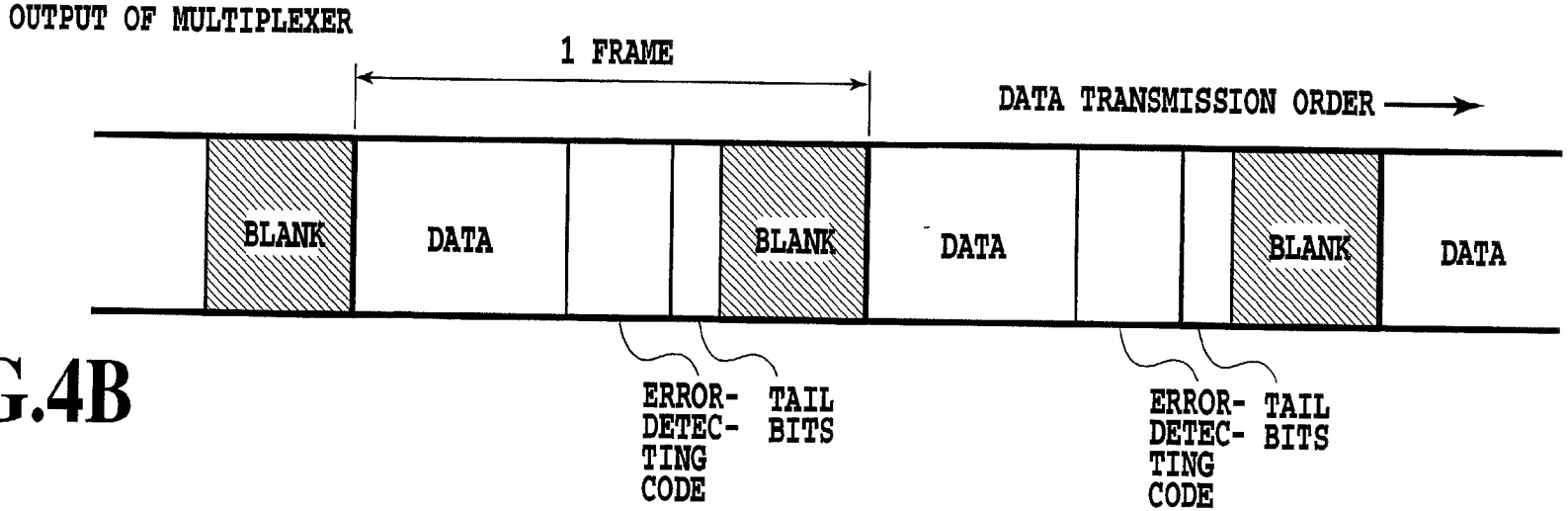

OUTPUT OF MULTIPLEXER
1 FRAME
DATA TRANSMISSION ORDER
BLANK
DATA
BLANK
DATA
BLANK
DATA
ERROR-DETEC-TING CODE
TAIL BITS
ERROR-DETEC-TING CODE
TAIL BITS

FIG.4B

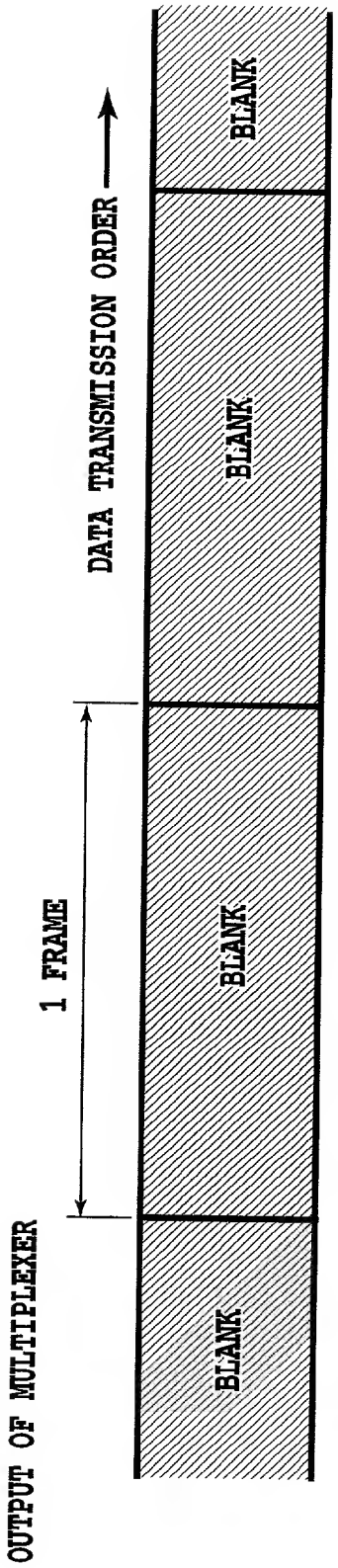

OUTPUT OF MULTIPLEXER
1 FRAME
DATA TRANSMISSION ORDER
BLANK
BLANK
BLANK
BLANK

FIG.4C

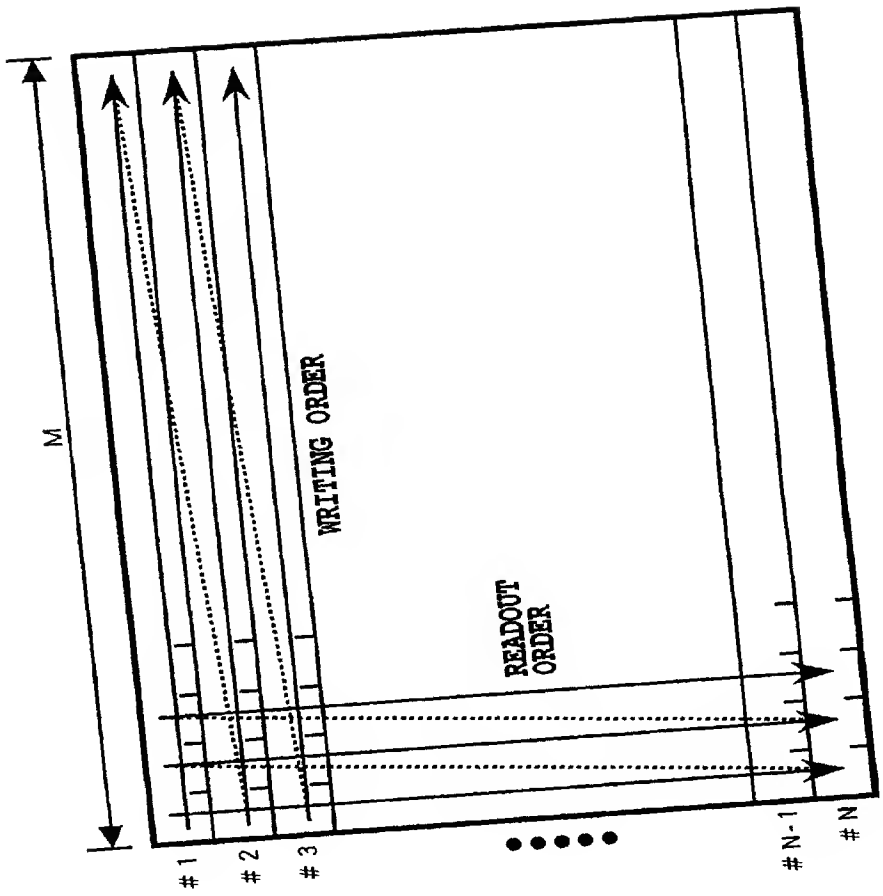


FIG.5

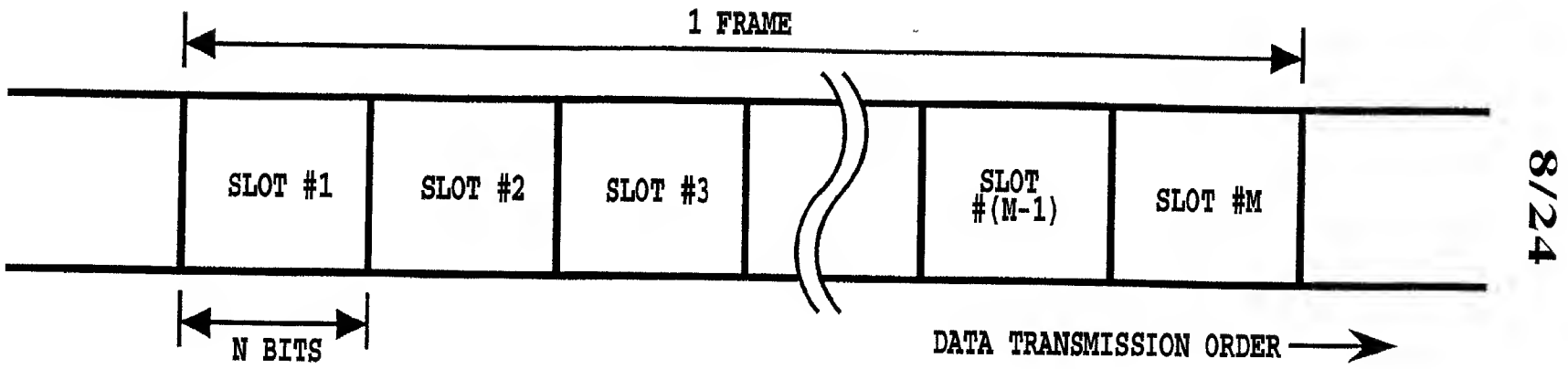

OUTPUT OF FRAME MEMORY
1 FRAME
SLOT #1
SLOT #2
SLOT #3
SLOT #(M-1)
SLOT #M
N BITS
DATA TRANSMISSION ORDER

FIG.6

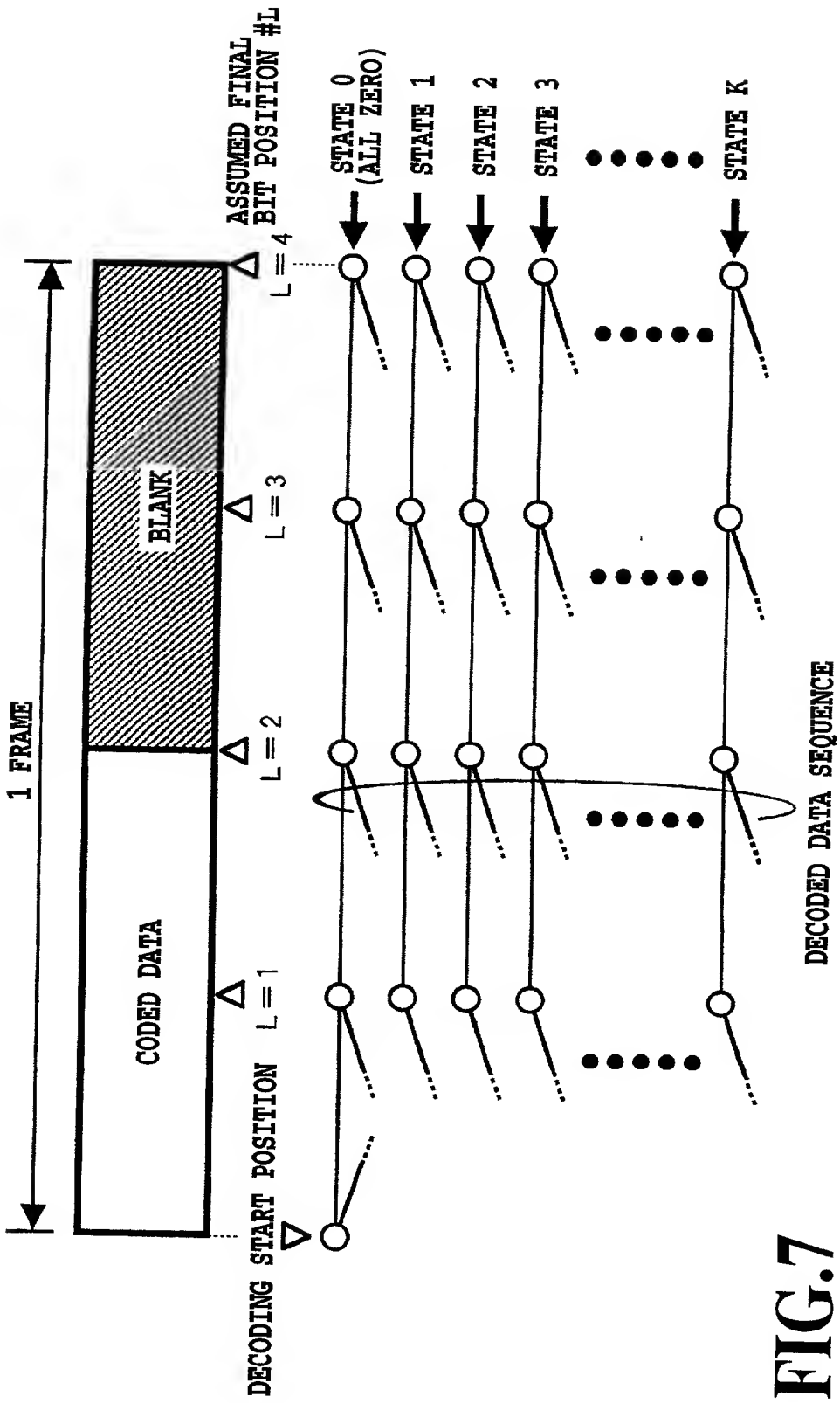

1 FRAME
CODED DATA
BLANK
DECODING START POSITION
L = 1
L = 2
L = 3
L = 4
ASSUMED FINAL BIT POSITION #L
STATE 0 (ALL ZERO)
STATE 1
STATE 2
STATE 3
STATE K
DECODED DATA SEQUENCE

FIG.7

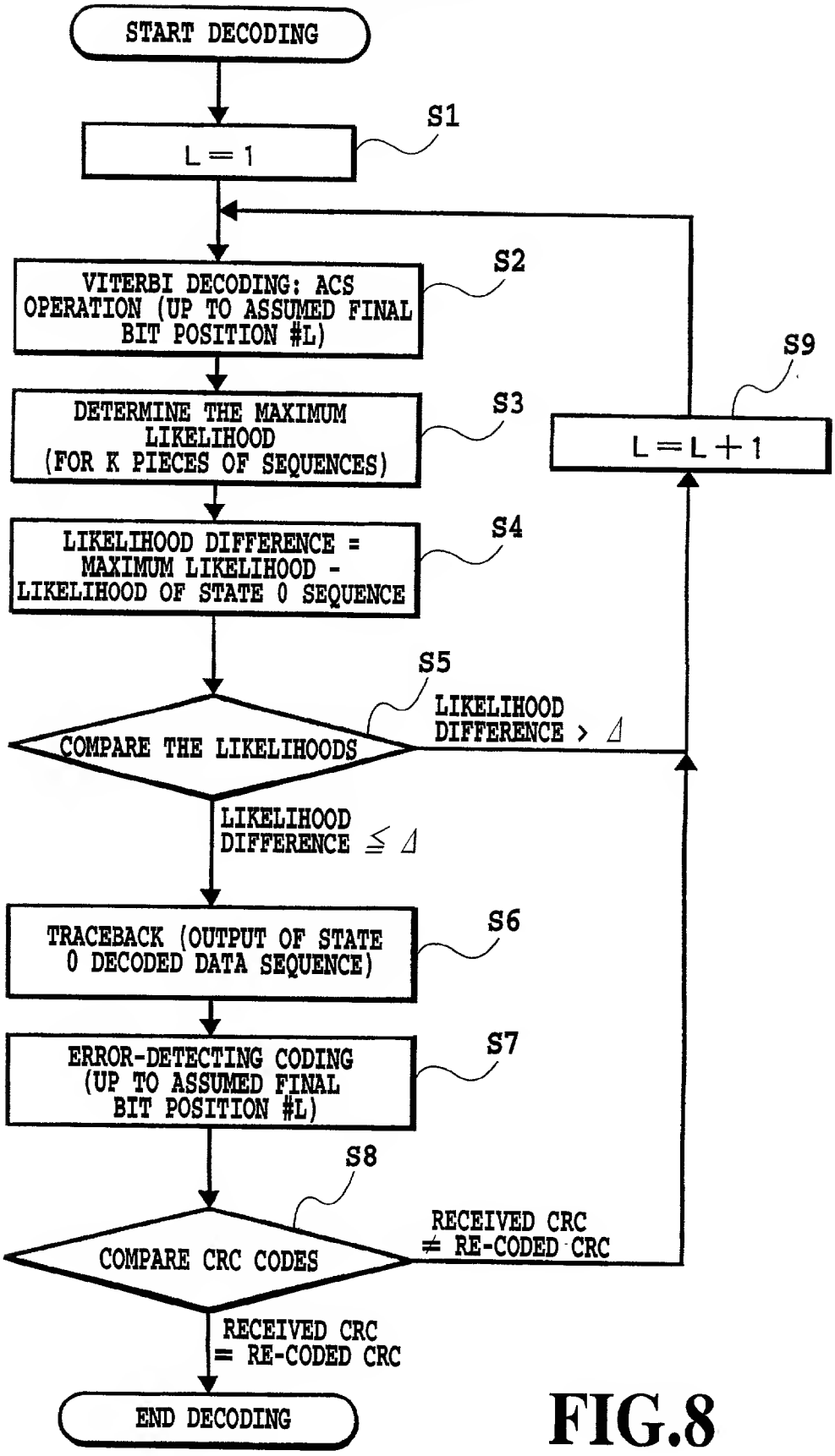

START DECODING
S1
L = 1
S2
VITERBI DECODING: ACS OPERATION (UP TO ASSUMED FINAL BIT POSITION #L)
S3
DETERMINE THE MAXIMUM LIKELIHOOD (FOR K PIECES OF SEQUENCES)
S4
LIKELIHOOD DIFFERENCE = MAXIMUM LIKELIHOOD - LIKELIHOOD OF STATE 0 SEQUENCE
S5
COMPARE THE LIKELIHOODS
LIKELIHOOD DIFFERENCE > Δ
LIKELIHOOD DIFFERENCE ≦ Δ
S9
L = L + 1
S6
TRACEBACK (OUTPUT OF STATE 0 DECODED DATA SEQUENCE)
S7
ERROR-DETECTING CODING (UP TO ASSUMED FINAL BIT POSITION #L)
S8
COMPARE CRC CODES
RECEIVED CRC ≠ RE-CODED CRC
RECEIVED CRC = RE-CODED CRC
END DECODING

FIG.8

FIG.9

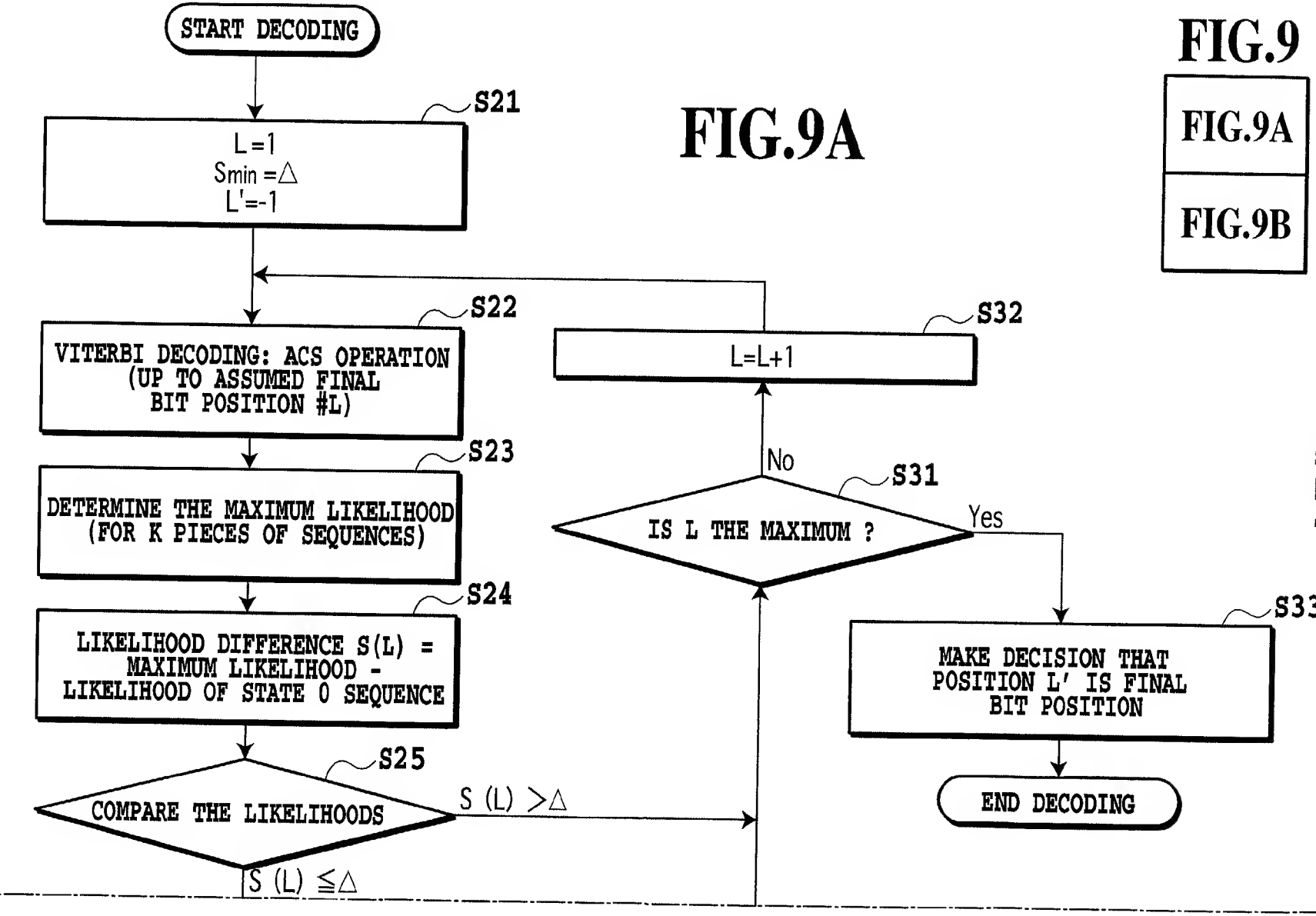


FIG.9A

FIG.9A
FIG.9B

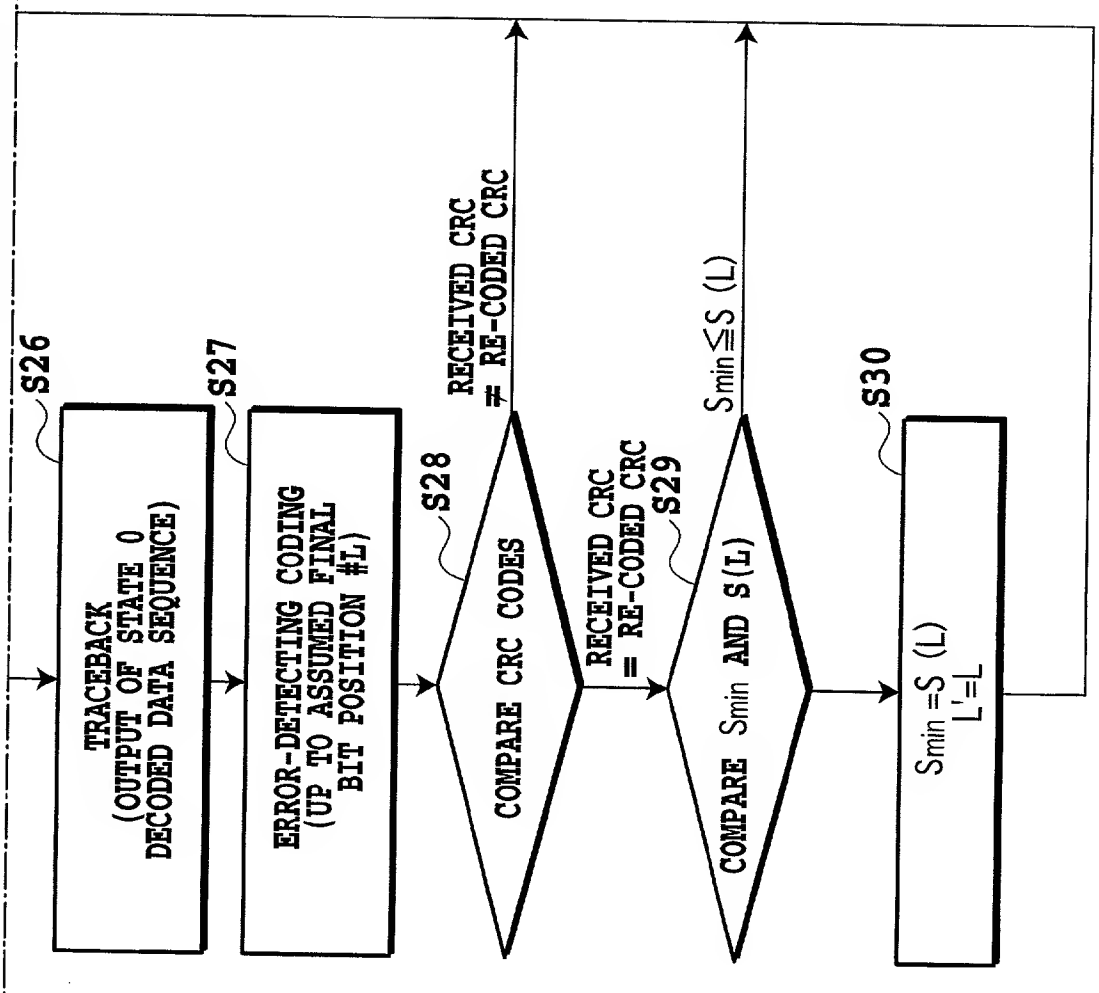
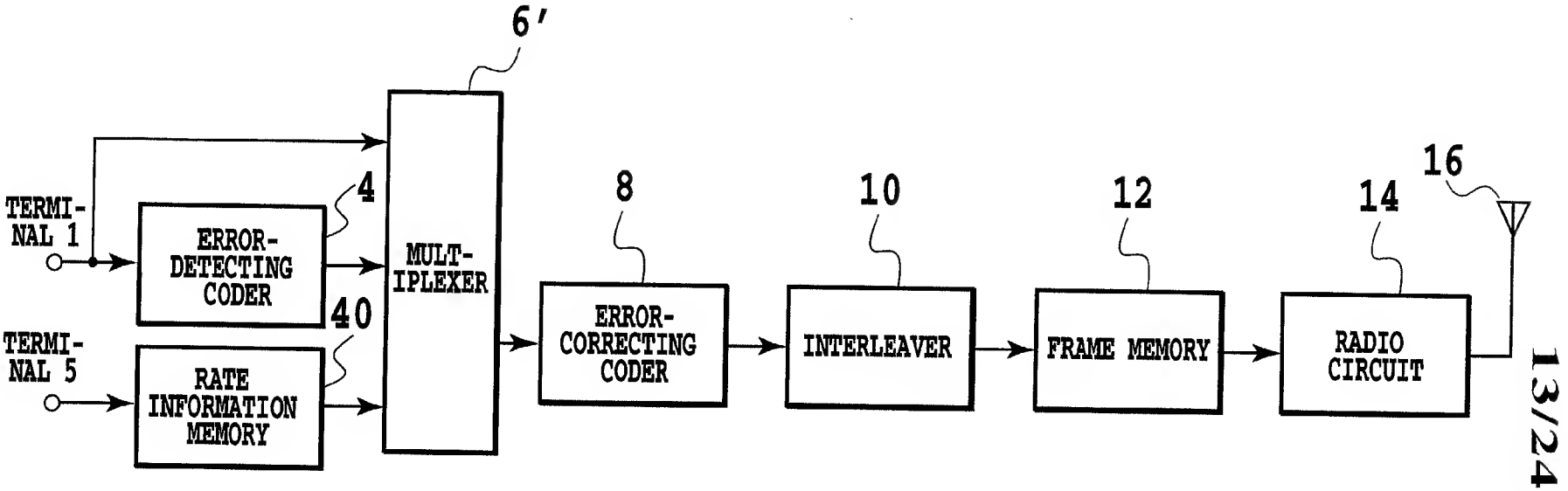
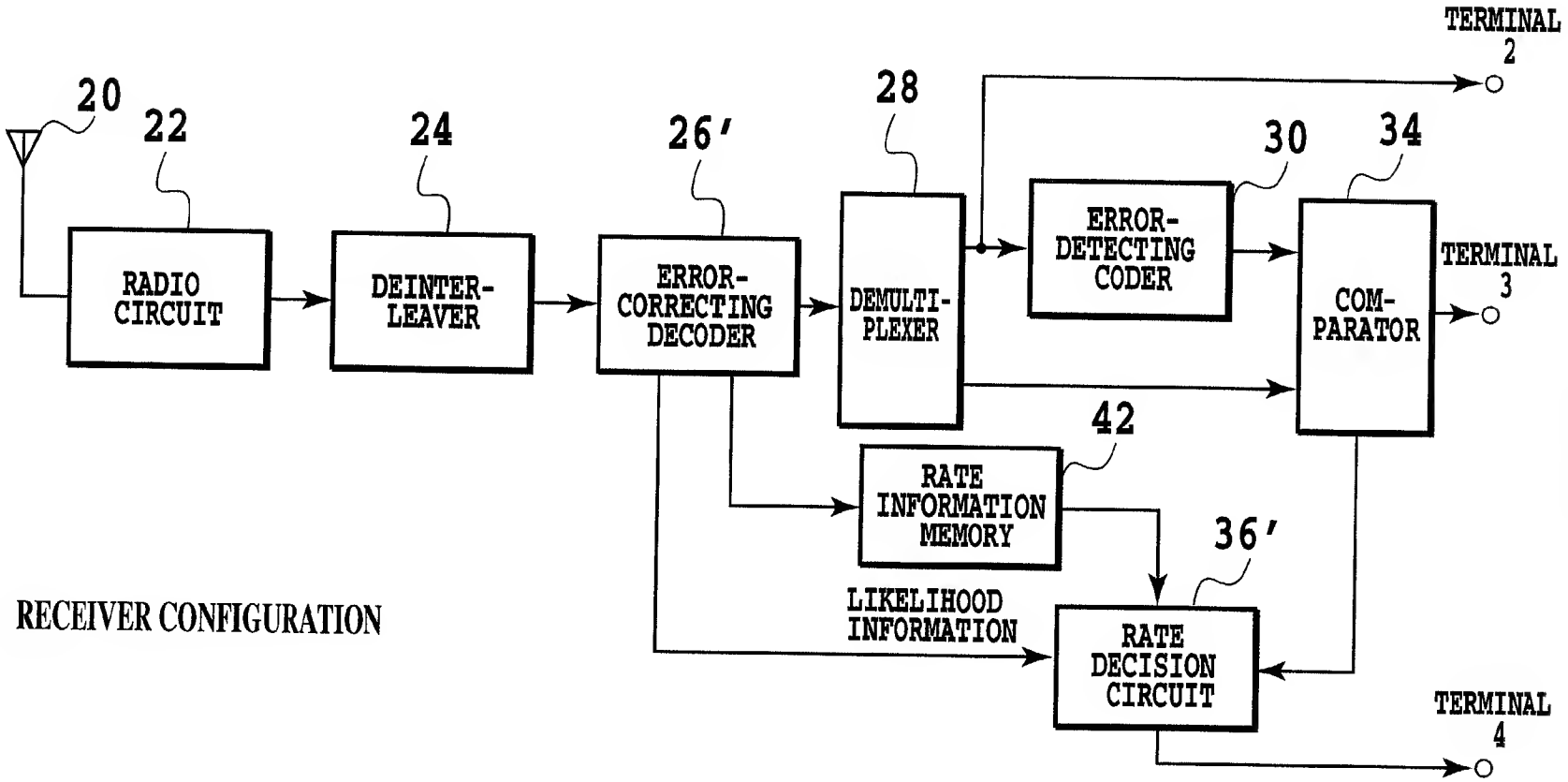

S26
TRACEBACK
(OUTPUT OF STATE 0
DECODED DATA SEQUENCE)
S27
ERROR-DETECTING CODING
(UP TO ASSUMED FINAL
BIT POSITION #L)
S28
COMPARE CRC CODES
RECEIVED CRC
≠ RE-CODED CRC
RECEIVED CRC
= RE-CODED CRC
S29
COMPARE Smin AND S(L)
Smin≦S (L)
S30
Smin =S (L)
L'=L

FIG.9B



TRANSMITTER CONFIGURATION

FIG.10A



RECEIVER CONFIGURATION

FIG.10B

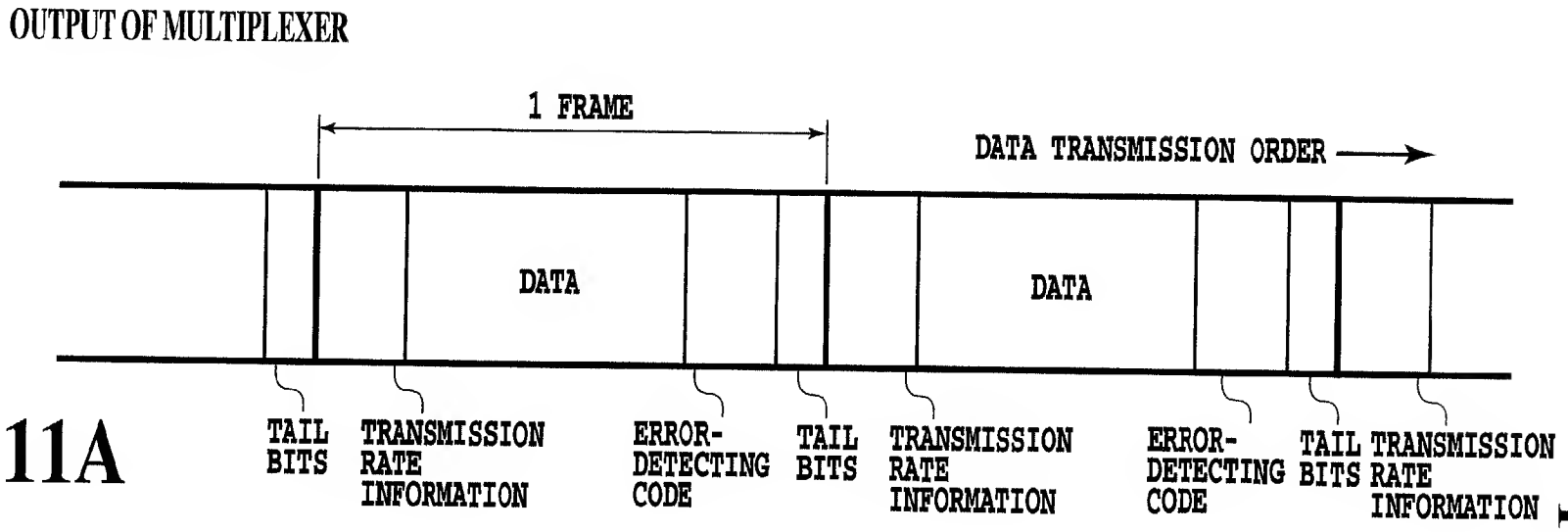


FIG.11A

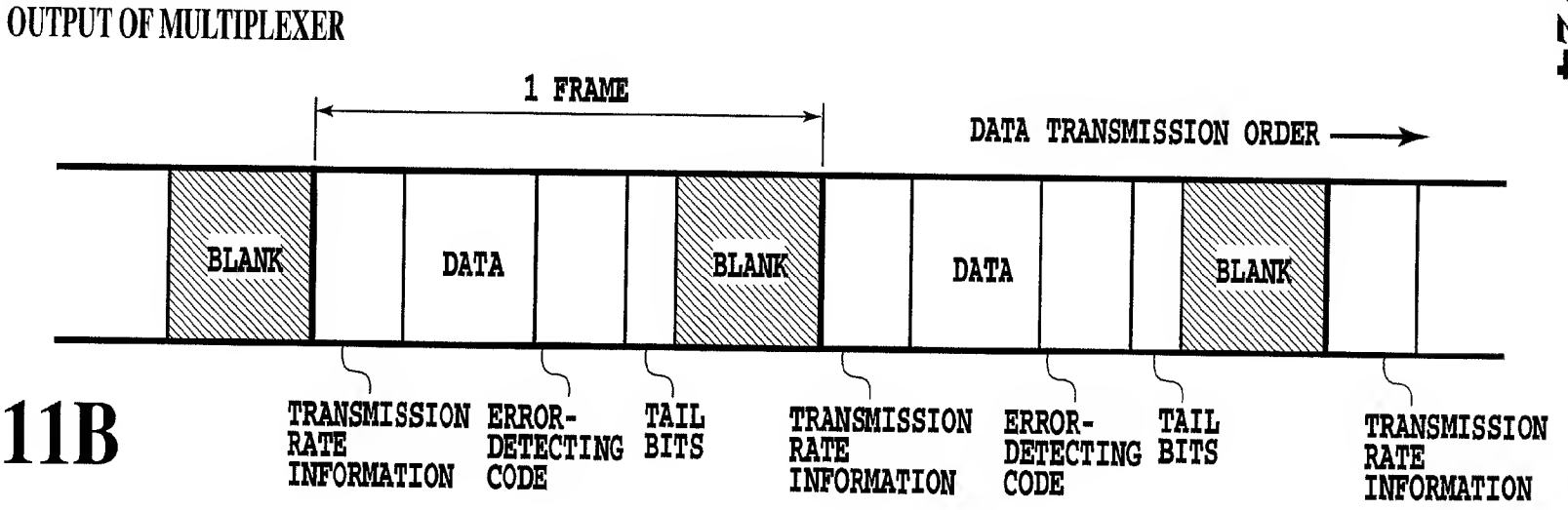


FIG.11B

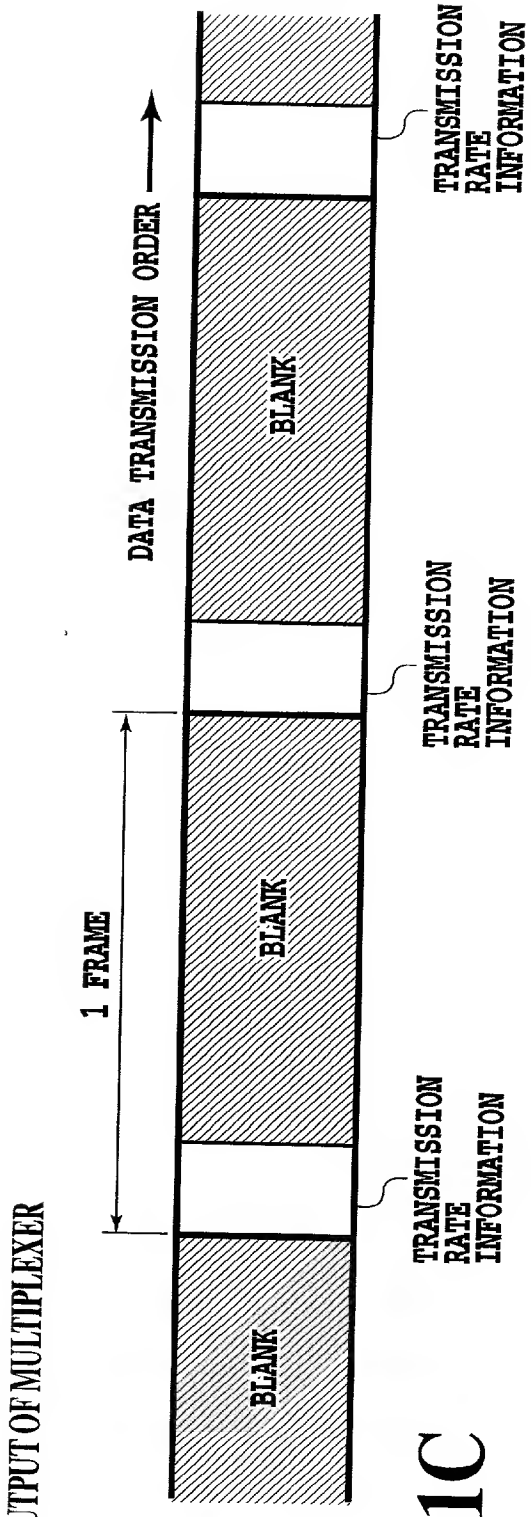

OUTPUT OF MULTIPLEXER
1 FRAME
DATA TRANSMISSION ORDER
BLANK
BLANK
BLANK
TRANSMISSION RATE INFORMATION
TRANSMISSION RATE INFORMATION
TRANSMISSION RATE INFORMATION

FIG.11C

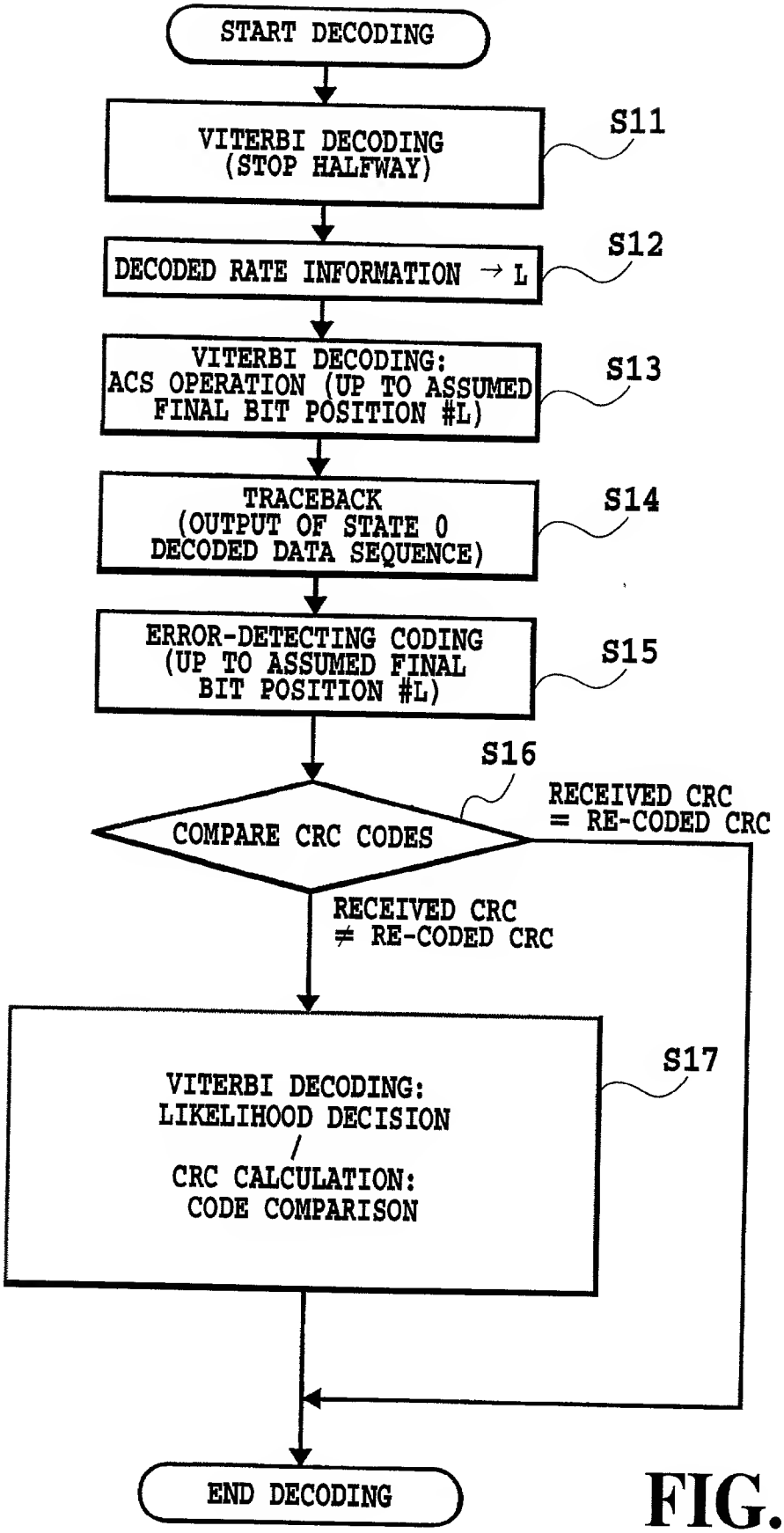

START DECODING
VITERBI DECODING (STOP HALFWAY)
S11
DECODED RATE INFORMATION → L
S12
VITERBI DECODING: ACS OPERATION (UP TO ASSUMED FINAL BIT POSITION #L)
S13
TRACEBACK (OUTPUT OF STATE 0 DECODED DATA SEQUENCE)
S14
ERROR-DETECTING CODING (UP TO ASSUMED FINAL BIT POSITION #L)
S15
S16
COMPARE CRC CODES
RECEIVED CRC = RE-CODED CRC
RECEIVED CRC ≠ RE-CODED CRC
VITERBI DECODING: LIKELIHOOD DECISION / CRC CALCULATION: CODE COMPARISON
S17
END DECODING

FIG.12

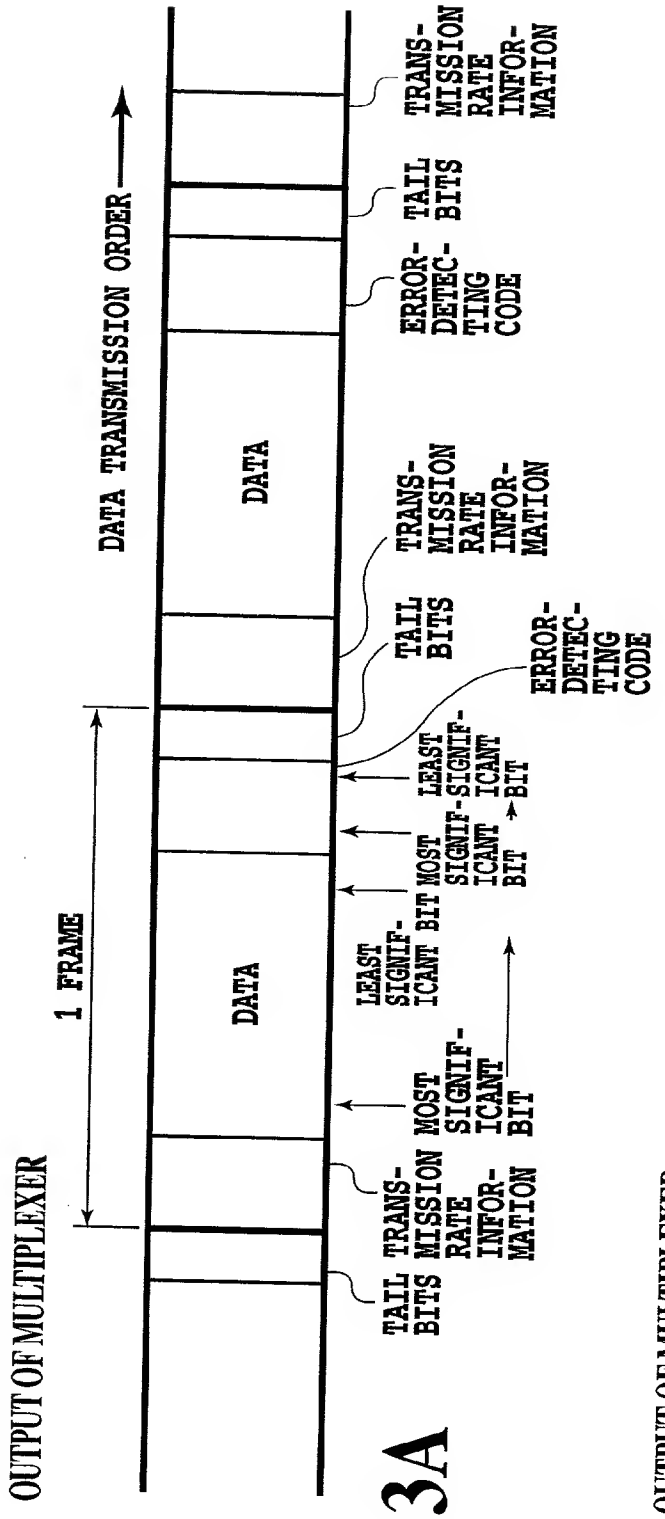


FIG.13A

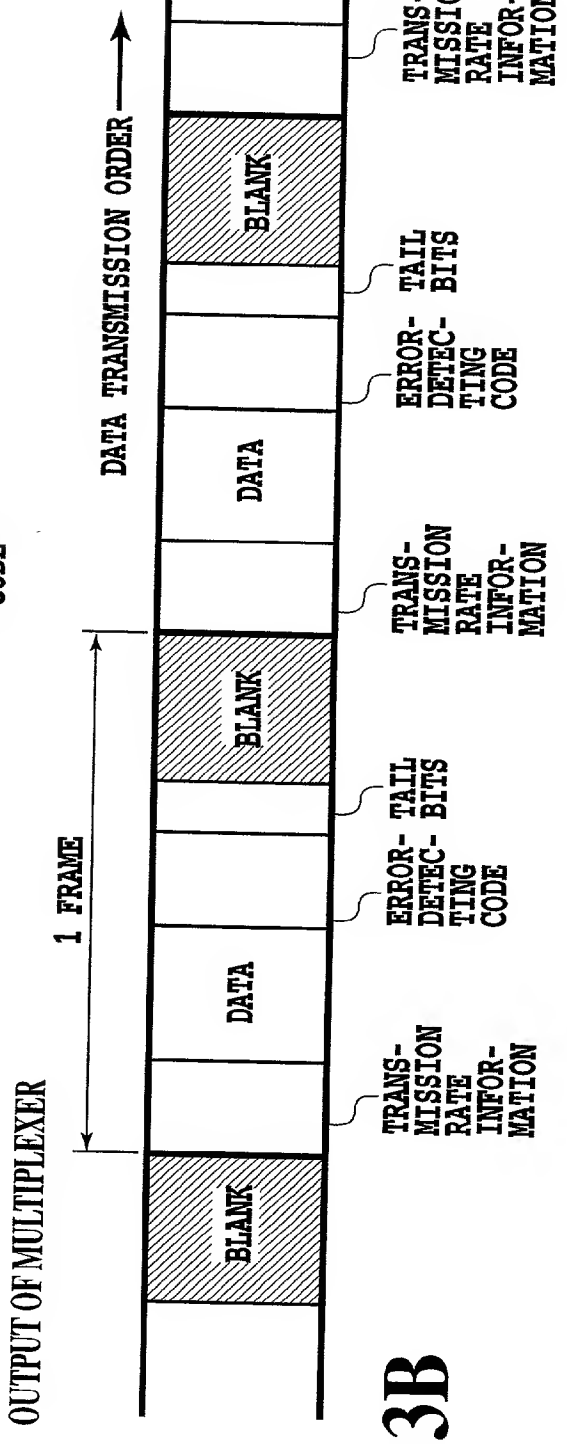


FIG.13B

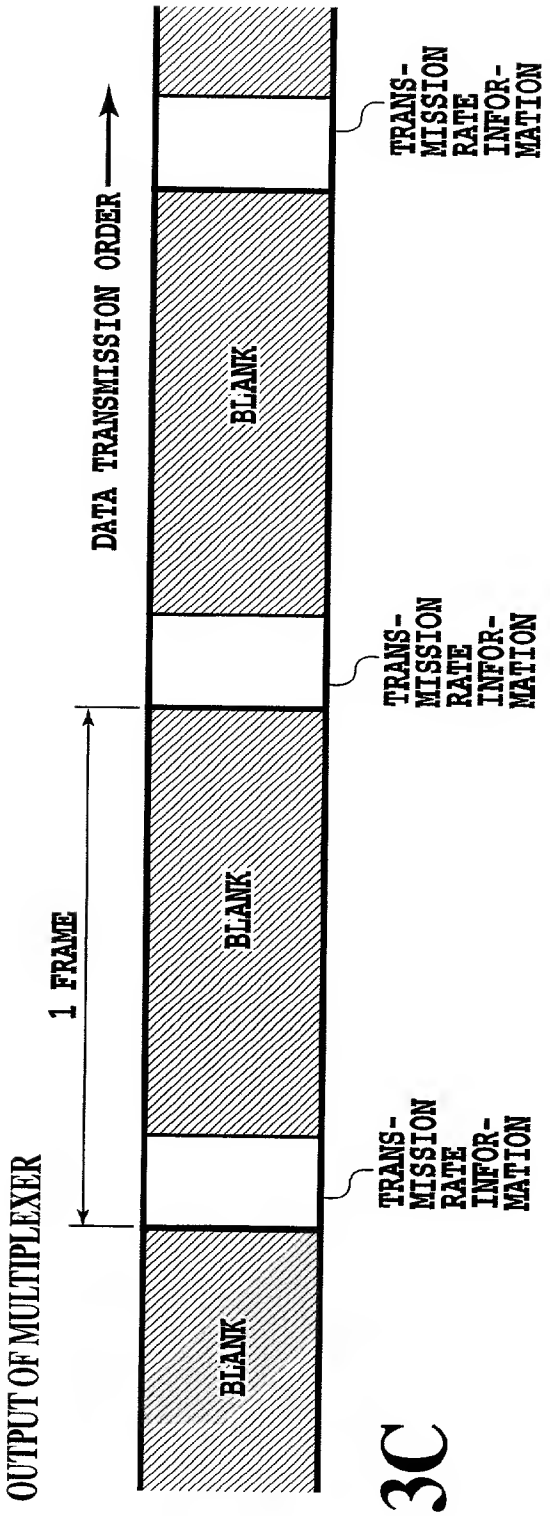

OUTPUT OF MULTIPLEXER
1 FRAME
DATA TRANSMISSION ORDER
BLANK
BLANK
BLANK
TRANS-MISSION RATE INFOR-MATION
TRANS-MISSION RATE INFOR-MATION
TRANS-MISSION RATE INFOR-MATION

FIG.13C

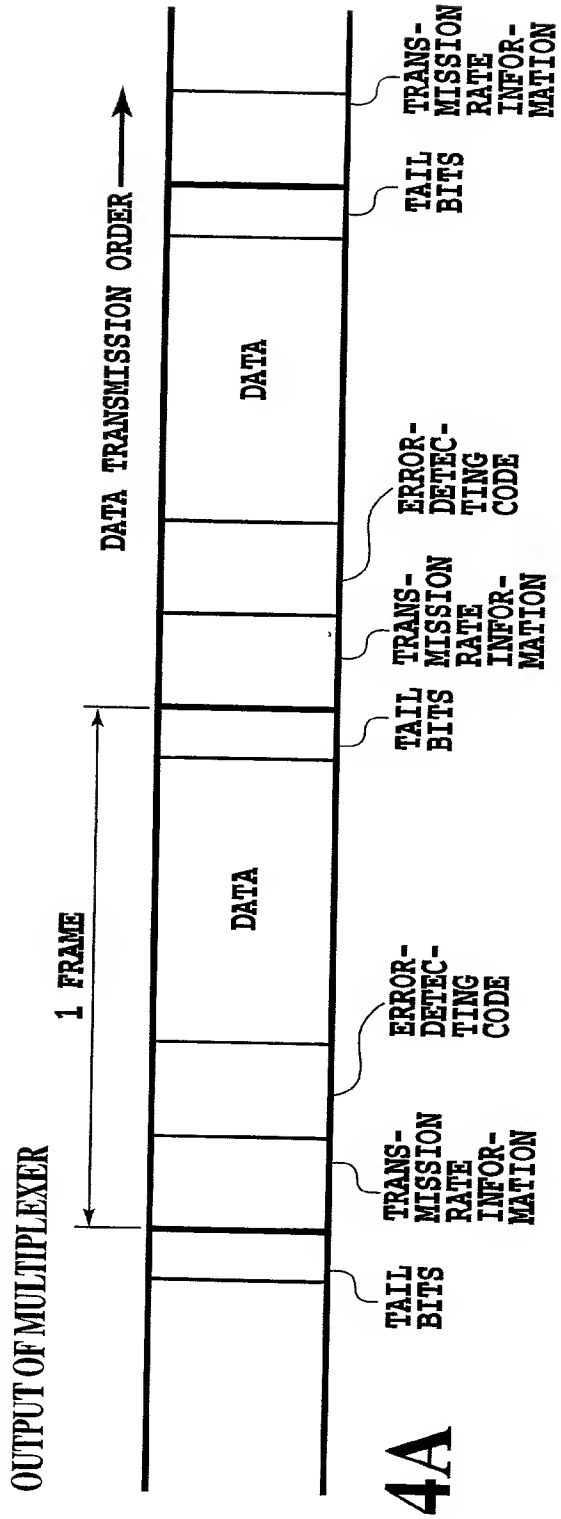


FIG.14A

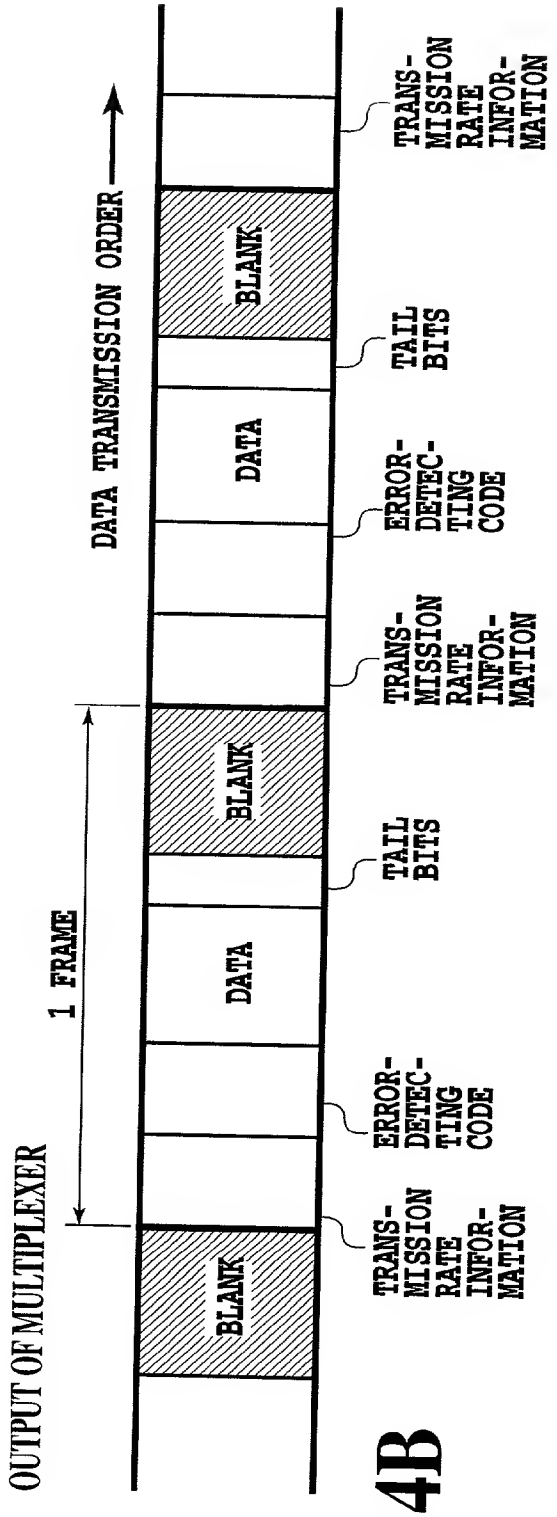


FIG.14B

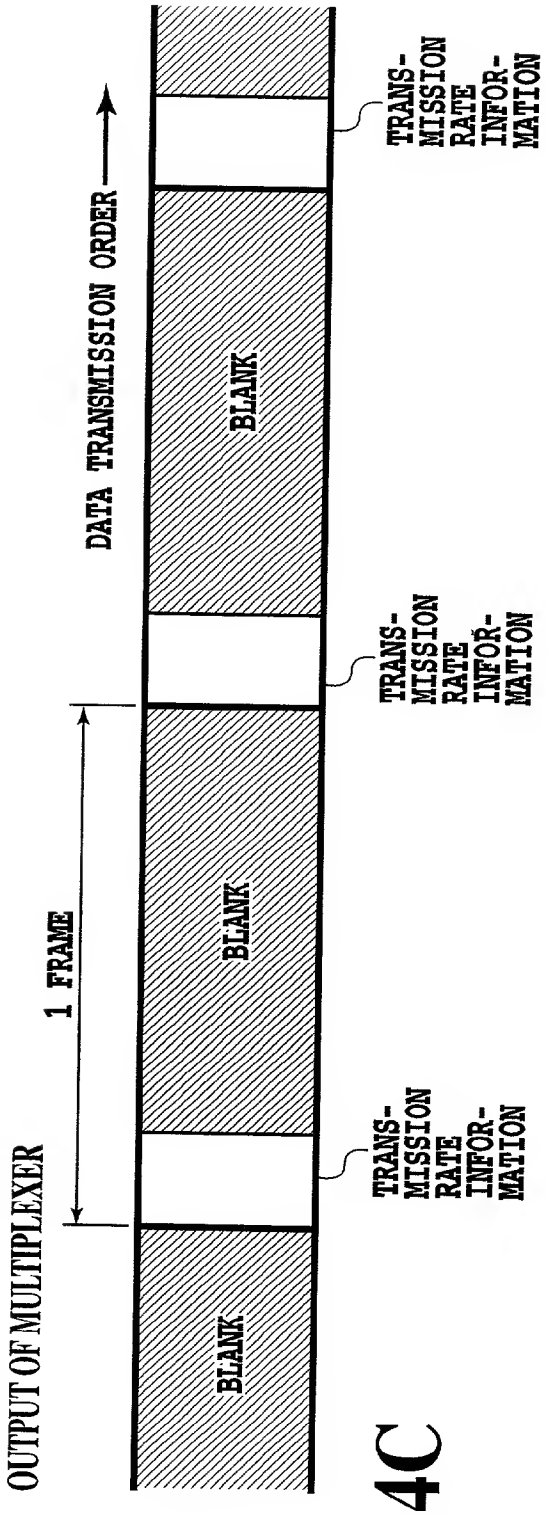

OUTPUT OF MULTIPLEXER
1 FRAME
DATA TRANSMISSION ORDER
BLANK
BLANK
BLANK
TRANS-
MISSION
RATE
INFOR-
MATION
TRANS-
MISSION
RATE
INFOR-
MATION
TRANS-
MISSION
RATE
INFOR-
MATION

FIG.14C

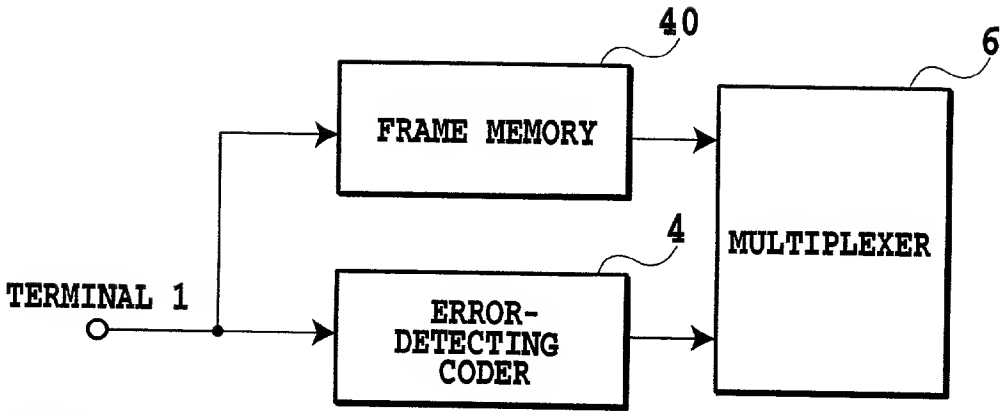


FIG.15A

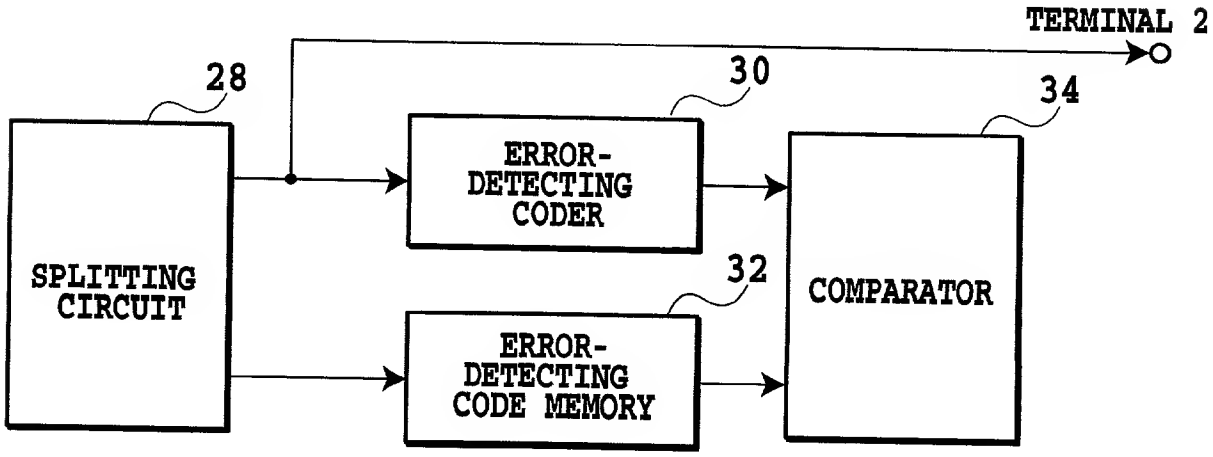


FIG.15B

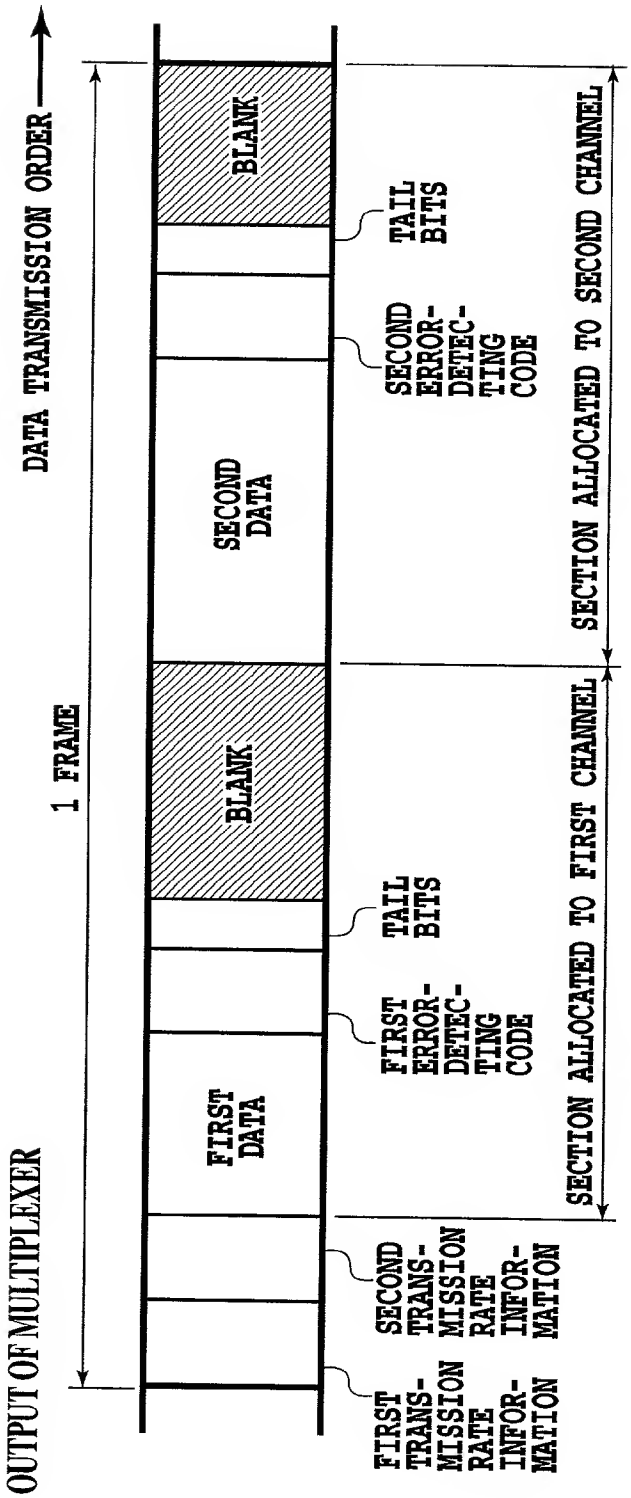

OUTPUT OF MULTIPLEXER
DATA TRANSMISSION ORDER
1 FRAME
FIRST TRANS-MISSION RATE INFOR-MATION
SECOND TRANS-MISSION RATE INFOR-MATION
FIRST DATA
BLANK
FIRST ERROR-DETEC-TING CODE
TAIL BITS
SECOND DATA
BLANK
SECOND ERROR-DETEC-TING CODE
TAIL BITS
SECTION ALLOCATED TO FIRST CHANNEL
SECTION ALLOCATED TO SECOND CHANNEL

FIG.16

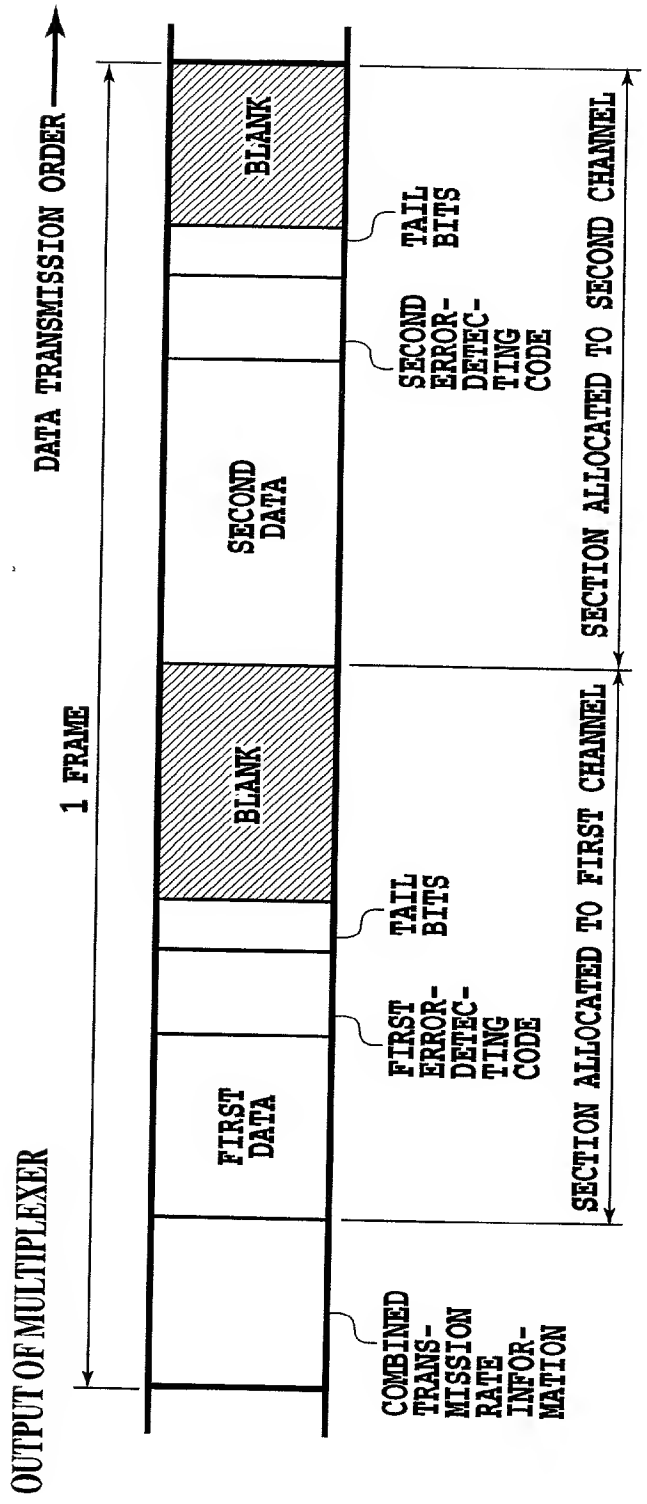

OUTPUT OF MULTIPLEXER
DATA TRANSMISSION ORDER
1 FRAME
COMBINED TRANS-MISSION RATE INFOR-MATION
FIRST DATA
FIRST ERROR-DETEC-TING CODE
TAIL BITS
BLANK
SECOND DATA
SECOND ERROR-DETEC-TING CODE
TAIL BITS
BLANK
SECTION ALLOCATED TO FIRST CHANNEL
SECTION ALLOCATED TO SECOND CHANNEL

FIG.17